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SUPPLY VOLTAGE, $+V_S$ to $-V_S$ SUPPLY VOLTAGE, $+V_B$ SUPPLY VOLTAGE, $-V_B$ OUTPUT CURRENT, peak POWER DISSIPATION, internal, DC INPUT VOLTAGE TEMPERATURE, pin solder, 10s TEMPERATURE, junction² TEMPERATURE RANGE, storage OPERATING TEMPERATURE, case 200V + V_S + 15V⁶ - V_S - 15V⁶ 12A, within SOA 100W + V_B to - V_B 225°C. 150°C. -40 to 105°C. -40 to 85°C.

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PARAMETER	TEST CONDITIONS ¹	MIN	MP108 TYP	МАХ	MIN	MP108A TYP	МАХ	UNITS
INPUT OFFSET VOLTAGE OFFSET VOLTAGE vs. temperature OFFSET VOLTAGE vs. supply BIAS CURRENT, initial ³ BIAS CURRENT vs. supply OFFSET CURRENT, initial INPUT RESISTANCE, DC INPUT CAPACITANCE COMMON MODE VOLTAGE RANGE COMMON MODE VOLTAGE RANGE COMMON MODE REJECTION, DC NOISE	Full temperature range 1MHz bandwidth, 1kΩ R _S	92	1 20 10 ¹¹ 4 10	5 50 20 100 0.1 50 +V _B - 15 -V _B + 15	*	* * * *	3 * 70 * 30 *	mV μV/°C μV/V pA pA/V pA Ω pF V V dB μV RMS
GAIN OPEN LOOP @ 15Hz GAIN BANDWIDTH PRODUCT @ 1MHz PHASE MARGIN	$R_L = 10K\Omega$, $C_C = 10pF$ $C_C = 10pF$ Full temperature range	96 45	10		*	*		dB MHz degrees
OUTPUT VOLTAGE SWING VOLTAGE SWING VOLTAGE SWING VOLTAGE SWING CURRENT, continuous, DC SLEW RATE, $A_V = -20$ SETTLING TIME, to 0.1% RESISTANCE POWER BANDWIDTH 180V _{P-P}	$\begin{split} I_{O} &= 10A \\ I_{O} &= -10A \\ I_{O} &= 10A, +V_{B} = +V_{S} + 10V \\ I_{O} &= -10A, -V_{B} = -V_{S} - 10V \\ C_{C} &= 10pF \\ 2V \ Step \\ No \ load, \ DC \\ C_{C} &= 10pF, +V_{S} = 100V, -V_{S} = -100V \end{split}$	+V _S - 10 -V _S + 10 +V _S - 1.6 -V _S + 5.1 10 150	+V _S - 8.6 -V _S + 7 170 1 5 300		* * * 11 *	* * * *		V V V Α V/μS μS Ω kHz
POWER SUPPLY VOLTAGE CURRENT, quiescent		±15	±75 50	±100 65	*	*	*	V mA
THERMAL RESISTANCE, AC, junction to case ⁵ RESISTANCE, DC, junction to case RESISTANCE, junction to air TEMPERATURE RANGE, case	Full temperature range, $f \le 60Hz$ Full temperature range, $f < 60Hz$ Full temperature range	-40		1 1.25 13 85	*		* * *	°C/W °C/W °C/W °C

NOTES: 1. Unless otherwise noted: T_C=25°C, compensation C_C=100pF, DC input specifications are value given, power supply voltage is typical rating.

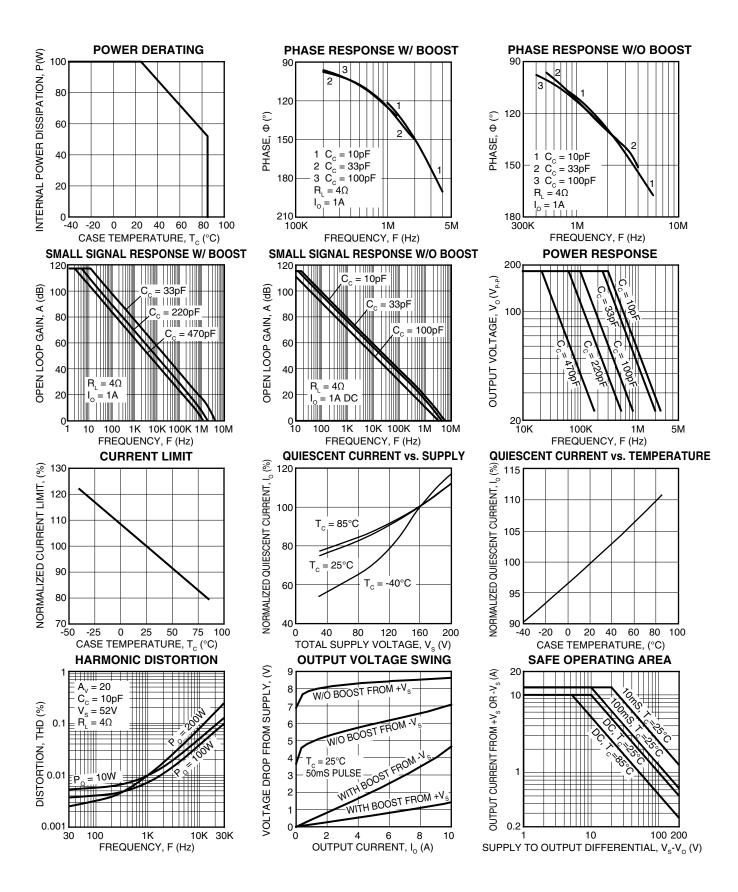
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.

3. Doubles for every 10°C of case temperature increase.

4. +V_S and -V_S denote the positive and negative supply voltages to the output stage. +V_B and -V_B denote the positive and negative supply voltages to the input stages.

5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

6. Power supply voltages +V_B and -V_B must not be less than +V_S and -V_S respectively.





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Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.cirrus.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Precision Power's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

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The MP108 has two ground pins (pins 3, 32). These pins provide a return for the internal capacitive bypassing of the small signal portions of the MP108. The two ground pins are **not** connected together on the substrate. Both of these pins are required to be connected to the system signal ground.

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The MOSFET output stage of the MP108 is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph on previous page). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

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The external compensation capacitor C_C is connected between pins 5 and 6. Unity gain stability can be achieved with any capacitor value larger than 100pF for a minimum phase margin of 45 degrees. At higher gains more phase shift can usually be tolerated in most designs and the compensation capacitor value can be reduced resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C for the application. An NPO (COG) type capacitor is required rated for the full supply voltage (200V).

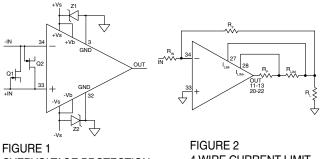
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Although the MP108 can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 signal diodes connected anti-parallel across the input pins is sufficient. In more demanding applications where bias current is important diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to ±0.7V. This is usually sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

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Bypass capacitors to power supply terminals $+V_{S}$ and $-V_{S}$ must be connected physically close to the pins to prevent local

parasitic oscillation in the output stage of the MP108. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater. In most applications power supply terminals $+V_B$ and $-V_B$ will be connected to $+V_S$ and -V_S respectively. Supply voltages +V_B and -V_B are bypassed internally but both ground pins 3 and 32 must be connected to the system signal ground to be effective. In all cases power to the buffer amplifier stage of the MP108 at pins 8 and 25 must be connected to +V_B and -V_B at pins 4 and 30 respectively. Provide local bypass capacitors at pins 8 and 25. See the external connections diagram on page 1.



OVERVOLTAGE PROTECTION **Ø33Ø5-*.*5**

4 WIRE CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 28 must be connected to the amplifier output side and pin 27 connected to the load side of the current limit resistor R_{LIM} as shown in Figure 2. This connection will bypass any parasitic resistances RP, formed by socket and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 2. The value of the current limit resistor can be calculated as follows: $R_{LIM} = .65/I_{LIMIT}$

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With the boost feature the small signal stages of the amplifier are operated at a higher supply voltages than the amplifierís high current output stage. $+V_B$ (pins 4,8) and $-V_B$ (pins 25,30) are connected to the small signal stages and +V_S (pins 14-16) and -V_S (pins 17-19) are connected to the high current output stage. An additional 10V on the $+V_B$ and $-V_B$ pins is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required. When the boost feature is not needed +V_S and -V_S are connected to the +V_B and -V_B pins respectively. The $+V_B$ and $-V_B$ pins must not be operated at supply voltages less than $+V_S$ and $-V_S$ respectively.

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The substrate of the MP108 is an insulated metal substrate. It is required that it be connected to signal ground. Connect pin 2 (back plate) to signal ground. The back plate will then be AC grounded to signal ground through a 1µF capacitor.

CONTACTING CIRRUS LOGIC SUPPORT

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